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3     What is claimed is:

4       1. A method of forming a semiconductor device comprising:

6           a) forming a gate structure over a substrate being doped with a first conductivity type  
7                      impurity;

8           b) performing a doped depletion region implantation by implanting ions being the  
9                      second conductive type to the substrate to form doped depletion regions  
10                  beneath and separated from said source/drain regions;

11           c) performing a S/D implant by implanting ions having a second conductivity type  
12                  into the substrate to form S/D regions adjacent to said gate;

13                  (1) said doped depletion regions have an impurity concentration and thickness  
14                      so that said doped depletion regions are depleted due to a built-in  
15                      potential created between said doped depletion regions and said  
16                      substrate.

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18       2. The method of claim 1 wherein doped depletion region are not formed under said gate  
19              structure.

20       3. The method of claim 1 which further includes said doped depletion regions have a  
21              impurity concentration so that the built-in junction potential between said doped depletion  
22              regions and said substrate forms depletion regions in the substrate between the  
23              source/drain regions and the doped depletion region;

1                   said depletion regions have a net impurity concentration of the first  
2 conductivity type.

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4     4. The method of claim 1 which further includes said doped depletion regions have a  
5     impurity concentration so that the built-in junction potential between said doped depletion  
6     regions and said substrate forms depletion regions in the substrate between the  
7     source/drain regions and the doped depletion region;        said depletion regions have a  
8     net impurity concentration of the first conductivity type;

9                   said depletion regions have a net impurity concentration between 1E16  
10    to 5E18 atom/cc.

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12     5. The method of claim 1 which further includes implanting ions of a first impurity type  
13    into said substrate between said source/drain regions and said doped depletion regions.

14     6. The method of claim 1 which further includes performing an implant type selected from  
15    the group consisting of Halo implant, threshold voltage implant, and a field implant, that  
16    implant ions of a first impurity type into said substrate at least between said source/drain  
17    regions and said doped depletion regions.

18     7. The method of claim 1 wherein the region of said substrate between said source/drain  
19    regions and said doped depletion regions has a concentration of a first type impurity  
20    between 1E16 to 1E18 atom/cc;  
21    a channel region in said substrate under said gate structure; said channel region has a  
22    concentration of a second type impurity between 1E16 to 1E18 atom/cc.

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1       16. The method of claim 1 wherein the LDD implantation is performed by implanting As  
2       ions at a dose between 5E14 and 1E16 atoms /cm<sup>2</sup>, at an energy between 1keV and 10  
3       keV.

4       17. The method of claim 1 wherein the LDD implantation is performed by implanting  
5       Boron ions at a dose between 1E14 and 5E15 atoms /cm<sup>2</sup>, at an energy between 1 keV  
6       and 10 keV.

7       18. The method of claim 1 wherein the doped depletion region implantation is performed  
8       by implanting As or P ions at a does between 5E12 and 5E13 atoms/cm2, at an energy  
9       between 100 keV and 500 keV; said doped depletion region has a minimum depth below  
10      the substrate surface between 0.09 and 0.7  $\mu\text{m}$ .

11      19. The method of claim 1 wherein the doped depletion region implantation is performed  
12      by implanting boron ions at a does between 5E11 and 5E13 atoms/cm2, at an energy  
13      between 50 keV and 200 keV; said doped depletion region has a minimum depth below  
14      the substrate surface between 0.09 and 0.7  $\mu\text{m}$ .

15      20. The method of claim 1 wherein the S/D implant is performed by implanting arsenic  
16      (As) or phosphorus (P) ions at a dose between 5E14 to 1E16 atoms/cm<sup>2</sup>, at an energy  
17      between 50 keV and 80 keV; said Source/drain regions have a depth below the substrate  
18      surface of between 0.04 and 0.5  $\mu\text{m}$ .

19      21. The method of claim 1 wherein said second conductivity type is p-type; and said S/D  
20      implant is performed by implanting boron ions at a dose between 5E14 to 1E16  
21      atoms/cm<sup>2</sup>, at an energy between 50keV and 80keV; said source/drain regions have a depth  
22      below the substrate surface of between 0.04 and 0.5  $\mu\text{m}$ .

23      22. The method of claim 1 which further includes forming one or more spacers on the  
24      sidewalls of said gate structure.

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2 23. A method of forming a semiconductor device comprising:

3       a) forming a gate structure over on substrate being doped with a first conductivity

4           type impurity;

5       b) performing a doped depletion region implantation by implanting ions being the

6           second conductive type to the substrate to form doped depletion regions

7           beneath and separated from said source/drain regions;

8           (1) said doped depletion regions have an impurity concentration and thickness

9                   so that said doped depletion regions are depleted due to a built-in

10                  potential created between said doped depletion regions and said

11                  substrate;

12           (2) said doped depletion regions have a impurity concentration so that the

13                  built-in junction potential between said doped depletion regions

14                  and said substrate forms depletion regions in the substrate between

15                  the source/drain regions and the doped depletion region; said

16                  depletion regions have a net impurity concentration of the first

17                  conductivity type; said depletion regions have a net impurity

18                  concentration between 1E16 to 1E18 atom/cc;

19       c) performing a S/D implant by implanting ions having a second conductivity type

20                  into the substrate to form S/D regions adjacent to said gate;

21           (1) said substrate between said source/drain regions and said doped depletion

22                  regions has a concentration of a first type impurity between 1E16 to

23                  1E18 atom/cc.

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- 1        24. The method of claim 23 wherein doped depletion region are not formed under said
  - 2        gate structure.
  - 3        25. The method of claim 23 wherein the region of said substrate between said source/drain
  - 4        regions and said doped depletion regions has a concentration of a first type impurity
  - 5        between 1E16 to 1E18 atom/cc;
  - 6        a channel region in said substrate under said gate structure; said channel region has a
  - 7        concentration of a second type impurity between 1E16 to 1E18 atom/cc.
  - 8        26. The method of claim 23 which further includes forming one or more spacers on the
  - 9        sidewalls of said gate structure.
  - 10      27. The method of claim 23 which further includes forming two or more spacers on the
  - 11      sidewalls of said gate structure prior to the doped depletion region implantation.
- 12
- 13      28. A semiconductor device comprising:
    - 14                  a semiconductor substrate having a surface; said semiconductor
    - 15                  substrate being doped with a first conductivity type impurity; the top portion of said
    - 16                  semiconductor substrate is comprised of a first doped layer of a first conductivity type;
    - 17                  a gate structure over the surface of said semiconductor substrate; said
    - 18                  gate structure comprising a gate dielectric layer and a gate electrode;
    - 19                  source/drain regions in said semiconductor substrate to oppose each
    - 20                  other with a channel region laterally residing therebetween at a location immediately
    - 21                  beneath said gate structure,

1                   doped depletion regions of a second conductivity type in said a first  
2       doped layer of a first conductivity type under said source/drain regions;

3                   doped depletion regions are determined in impurity concentration and  
4       thickness to ensure that this layer is fully depleted due to a built-in potential creatable  
5       between said substrate and doped depletion regions;

6                   whereby said doped depletion regions reduce the capacitance between  
7       the source/drain regions and the substrate.

8       29. The semiconductor device of claim 28 which further includes said doped depletion  
9       regions under said source/drain regions, but not under said channel region.

10      30. The semiconductor device of claim 28 which further includes LDD regions that extend  
11     from said source/drain regions toward said channel region; said LDD regions being lower  
12     in impurity concentration and shallower in depth than said source/drain region.

13      31. The semiconductor device of claim 28 which further includes depletion regions and  
14     S/D depletion regions adjacent said doped depletion regions and between said  
15     source/drain regions: and

16                   said doped depletion regions and; said depletion regions have a net  
17     impurity concentration of the first conductivity type.

18      32. The semiconductor device of claim 28 which further includes depletion regions  
19     between said source/drain regions and said doped depletion regions; said depletion regions  
20     have a net impurity concentration of the first conductivity type; said depletion regions has  
21     a net impurity concentration between 1E16 to 1E18 atom/cc..

1       33. The semiconductor device of claim 28 which further includes said doped depletion  
2       regions have a impurity concentration so that the built-in junction potential between said  
3       doped depletion regions and said substrate forms depletion regions in the substrate  
4       between the source/drain regions and the doped depletion region;

5                         said depletion regions have a net impurity concentration of the first  
6       conductivity type.

7       34. The semiconductor device of claim 28 which further includes said doped depletion  
8       regions have a impurity concentration so that the built-in junction potential between said  
9       doped depletion regions and said substrate forms depletion regions in the substrate  
10      between the source/drain regions and the doped depletion region; said depletion regions  
11      have a net impurity concentration of the first conductivity type;

12                         said depletion regions have a net impurity concentration between 1E16  
13      to 1E18 atom/cc.

14       35. The semiconductor device of claim 28 which further includes one or more spacers on  
15      the sidewalls of said gate structure.